REMARKS

By the present Amendment, Applicant amends claims 1 and 2. Claims 1, 2, 7, 9, 11, 13, and 15 are pending in this application.

In the non-final Office Action mailed April 16, 2009¹, the Examiner rejected claims 1, 2, 7, 9, 11, 13, and 15 under 35 U.S.C. § 103(a) as unpatentable over U.S. Patent No. 5,994,762 to Suwanai et al. ("Suwanai") in view of Stanley Wolf et al., "Silicon Processing for the VLSI Era," 2000, Volume 1, Lattice Press, 719-727, 791-795 ("Wolf"), and further in view of U.S. Patent No. 6,770,977 to Kishida et al. ("Kishida"). Applicant respectfully traverses the rejection because the claims as amended are not obvious over the cited references.

The key to supporting any rejection under 35 U.S.C. § 103 is the clear articulation of the reason(s) why the claimed invention would have been obvious. Such an analysis should be made explicit and cannot be premised upon mere conclusory statements. See M.P.E.P. § 2142, 8th Ed., Rev. 6 (Sept. 2007). "A conclusion of obviousness requires that the reference(s) relied upon be enabling in that it put the public in possession of the claimed invention." M.P.E.P. § 2145.

It would not have been obvious for one of ordinary skill to combine the teachings of <u>Suwanai</u>, <u>Wolf</u>, and <u>Kishida</u> to obtain a semiconductor device comprising, *inter alia*, "a first insulating film formed above the semiconductor substrate and having a relative dielectric constant of 3.8 or less" and "a second insulating film covering the outer side face of the conductor and having a relative dielectric constant of over 3.8, at least a part

¹ The non-final Office Action contains a number of statements reflecting characterizations of the related art and the claims. Regardless of whether any such statement is identified herein, Applicant declines to automatically subscribe to any statement or characterization in the non-final Office Action.

of the second insulating film being formed at a same distance from the semiconductor substrate as a part of the first insulating film." Even the combination of teachings from Suwanai, Wolf, and Kishida that was suggested by the non-final Office Action fails to include that "the first insulating film and the second insulating film are positioned so as to directly sandwich the conductor at least at a first horizontal level above the semiconductor substrate and also at a second horizontal level higher than the first horizontal level above the semiconductor substrate," as recited in claim 1 (emphasis added).

Fig. 11 of <u>Suwanai</u>, which was relied upon in the non-final Office Action (see page 2, numbered paragraph 5), shows a device that includes a semiconductor substrate 1, a wiring 18 formed within a first BPSG (boron-doped phospho silicate glass) film 17, and a silicon oxide film 27. <u>Suwanai</u> at col. 7, line 66 to col. 8, line 4. <u>Suwanai</u> further shows a second BPSG film 20 formed above the wiring 18, the first BPSG film 17, and the silicon oxide film 27. <u>Id.</u> at col. 8, lines 25-27. The Office Action alleged that the first BPSG film 17, silicon oxide film 27, and silicon oxide film 28, taken together, correspond to the claimed "first insulating film," and that the second BPSG film 20 corresponds to the claimed "second insulating film." <u>Office Action</u> at page 2, numbered paragraph 5 (continued on page 3).

Even if the Office Action's allegations were correct, which Applicant does not concede, <u>Suwanai</u> nevertheless fails to teach or suggest that "the first insulating film and the second insulating film are positioned so as to directly *sandwich the conductor* at least at a *first* horizontal level above the semiconductor substrate and also at a *second*

horizontal level higher than the first horizontal level," as recited in claim 1 (emphasis added).

Applicants advise that, in <u>Suwanai</u>, the layer 28 inside the GR and only the layer 28 outside the GR are positioned so as to *directly* sandwich the conductor GR at a first horizontal level above the semiconductor substrate and also at a second horizontal level higher than the first horizontal level. The layer 20 inside the GR and only the layer 20 outside the GR are positioned so as to *directly* sandwich the conductor GR at a first horizontal level above the semiconductor substrate and also at a second horizontal level higher than the first horizontal level above the semiconductor substrate. In other words, the layer 28 and the layer 20 are *not* positioned so as to *directly* sandwich the conductor GR at a first horizontal level above the semiconductor substrate and also at a second horizontal level higher than the first horizontal level above the semiconductor substrate.

Wolf does not make up for the deficiencies of <u>Suwanai</u> because <u>Wolf</u> also fails to teach or suggest that "the first insulating film and the second insulating film are positioned so as to directly *sandwich the conductor* at least at a *first* horizontal level above the semiconductor substrate and also at a *second* horizontal level higher than the first horizontal level above the semiconductor substrate," as recited in claim 1 (emphasis added). The Office Action does not rely on <u>Wolf</u> for any teaching or suggestion of this limitation in claim 1.

Kishida fails to make up for the deficiencies of Suwanai and Wolf because

Kishida also does not teach or suggest that "the first insulating film and the second insulating film are positioned so as to directly sandwich the conductor at least at a first horizontal level above the semiconductor substrate and also at a second horizontal level

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higher than the first horizontal level," as recited in claim 1 (emphasis added). The Office

Action does not rely on Kishida for any teaching or suggestion of this limitation in claim

1.

The non-final Office Action's proposed combination of Suwanai, Wolf, and

Kishida fails to teach or suggest the semiconductor device recited in claim 1, and the

final Office Action has not identified any reason why one of ordinary skill would

otherwise modify Suwanai, Wolf, and Kishida, either individually or in combination, to

obtain the semiconductor device recited in claim 1. Thus, claim 1 and claims 2, 7, 9, 11,

13, and 15, which depend therefrom, are allowable over Suwanai, Wolf, and Kishida.

CONCLUSION

In view of the foregoing amendments and remarks, Applicant respectfully

requests reconsideration of this application and the timely allowance of the pending

claims.

Please grant any extensions of time required to enter this response and charge

any additional required fees to Deposit Account No. 06-0916.

Respectfully submitted,

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Dated: July 16, 2009

/Reece W. Nienstadt/

Reece Nienstadt

Reg. No. 52,072

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